# A New Switched-capacitor Inverter for Electric Vehicles

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## Abstract

*This paper presents a new switched-capacitor inverter circuit based on partial charging. A number of switched-capacitor inverter circuits have been developed, but most of them are based on switching of fully charged capacitors in specific sequence to generate staircase ac voltage. In order to reduce the output distortion, the numbers of capacitors and switches should be increased. However, complexity of the circuits will also be increased dramatically. Moreover, the number of capacitors of conventional switched-capacitor inverters should be limited, otherwise, the peak output voltage could exceed stipulated limit. The new switched-capacitor circuit operates in such a manner that the capacitors will be switched to generate an ac output while they are partially charged. Each capacitor can provide multilevel voltages because the state of charge is varied. Theoretically, ac voltage with unlimited steps can be created with a few of capacitors. Experiments and simulations of a thirteen-level inverter that consists of only two capacitors are included in this paper.*

## Keywords

*electric vehicle, inverter, switched- capacitor*

## 1. INTRODUCTION

With the advance of motor drive technologies, ac machines like induction motors are suitable for the propulsion systems of electric vehicles (EV) because they are rigid and require little maintenance. The main energy sources of EVs are batteries, and inverter can be employed to step up the dc voltage and generate an ac source. For the past decades, a number of switched-capacitor (SC) inverter topologies have been proposed. Most of the circuits are based on the principle of switching capacitors with fixed charge in specific sequence to create a staircase ac output. For some of the topologies like diode-clamped or capacitor-clamped SC, the capacitors will be connected in-series and be charged at a time. However, the voltages of all capacitors are the same, which are fraction of the input voltage. Thus, the peak magnitude of the ac output is limited. For other SC inverters like mixed-level hybrid multilevel cells and asymmetric hybrid multilevel cells topologies, separated dc sources are required for single-phase ac output. In general, the numbers of steps in the output voltage of the mentioned technologies are proportional to the number of cascaded capacitors. A large numbers of capacitors and switches are required to produce a sinusoidal waveform with acceptable distortion. Otherwise, complicated modulation strategies like carrier-based sinusoidal pulse width modulation (SPWM) should be employed [Axelrod et al., 2005; Park et al., 2003; Rodriguez et al., 2002; Marchesoni et al., 2002; Tolbert et al., 1999]. Certainly, ac voltage with minimal distortion is required by many equipment as well as motors of EVs because electronic devices like navigation system are susceptible to noise while harmonics lead to poor performance and greater energy loss of ac machines. A new SC multilevel inverter circuit based on partial charging is proposed. The capacitors will be switched while they are partially charged to different voltage levels. Thus, the number of steps in the output can be increased without increasing the number of cascade capacitors and switches. A prototype inverter that consists of only two capacitors with three levels of partial charging voltage is developed, which can generate thirteen levels of voltage with the peak ac doubled that of the input voltage. The results reveal that the output is closed to sinusoidal wave.

## 2. BASIC SC INVERTER

The basic operation of simple multilevel SC inverter circuits relies on the cascade of capacitors with fixed charge. Figure 1 and Figure 2 show the common charging topologies. The capacitors can be charged either in parallel or in-series. The number of steps is proportional to the number of capacitors and switches. For series charging topology, the capacitor voltage is less than the input voltage. Hence, the peak ac voltage can only be doubled that of the input voltage or even less. For parallel charging circuits, each capacitor will be charged to the same level of the input and the output voltage can be stepped up. It should be noted that the

stipulated peak voltage of the ac output limits the maximum number of capacitors of the parallel charging circuit. More capacitors can provide a smooth ac waveform, but the peak voltage will raise to such a level that damages loading equipment when all capacitors are in series. Input voltage, peak output voltage, harmonics and distortion are mutually dependent for both topologies. High frequency switching SPWM approach can solve the problem. However, capacitors with low equivalent series resistance should be employed. Otherwise, the switching losses of the capacitors are not negligible.

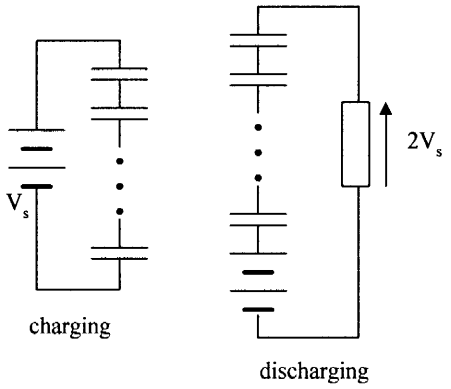



**Fig. 1** Inverter with capacitors charging in-series

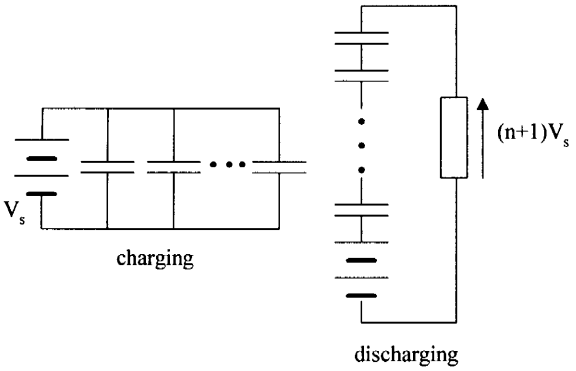



**Fig. 2** Inverter with capacitors charging in parallel

## 3. PROPOSED SC INVERTER

The proposed partially charged SC (PCSC) inverter is shown in Figure 3. The circuit can be divided into three sections. The first section consists of two switches and an inductor, namely $SW_a$, $SW_b$ and $L$. It is a combination of a buck and a boost converter that allows bi-directional energy flow. The buck converter operates to charge the capacitors during the first and third quarters of a cycle. The boost converter transfers the energy from the capacitors back to the source during second and fourth quarters of a cycle. The middle section is the core of the SC circuit. Two capacitors are employed to develop the prototype inverter. Actually, more capacitors can be included to boost up the peak output voltage. Each capacitor associates with a pair of switches so that it can be charged and discharged independently. The third switch connected between the two capacitors will be turned on and put them in-series for stepping up the output voltage. The output section consists of two pairs of switches, $SW_{O1}$, $SW_{O2}$, $SW_{O3}$ and $SW_{O4}$, which are responsible for changing the polarity of the output. Since the bi-directional converter and output bridge share all SCs, increasing the number of steps in the output can be achieved by putting more capacitors and switches to the middle section of the circuit only.

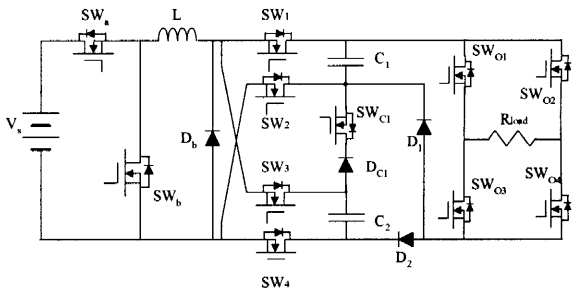



**Fig. 3** Proposed SC inverter

### *3.1 Modes of operation*

The circuit goes through eight modes of operation per cycle. The timing diagram of the output voltage and the gate pulse signal of the switches are shown in Figure 4. The switching topologies are shown in Figure 5.

***Mode 1***

This mode of operation starts from $t_0$ to $t_2$. Short duration pulses are applied to turn on $SW_a$ and $SW_2$ at $t_0$, $t_1$ and $t_2$. The durations of the three pulses are determined in such a manner that the output of the buck converter will be equal to $Vs/3$, $2Vs/3$ and $Vs$, respectively. Thus, the capacitor $C_1$ is charged with different voltage levels with charging current passing through $SW_2$ and the body diode of $SW_1$. $C_2$ does not receive any charge because $SW_4$ is off and $D_{C1}$ is reverse biased. Meanwhile, $SW_{O1}$ and $SW_{O2}$ are turned on and voltage across the load is positive.

***Mode 2***

Mode 2 starts at $t_3$ and pulses are applied to turn on $SW_a$ and $SW_4$ at $t_3$, $t_4$ and $t_5$. Likewise, $C_2$ is charged to three levels of voltages. $SW_{C1}$ will be turned on and connects the two capacitors in-series. Since $SW_1$ is off, no current can flow from $C_1$ toward the input source. The output voltage is equal to the sum of the voltages across $C_1$ and $C_2$.

***Mode 3***

$SW_b$ is turned on and the boost converter operates mode 3. $SW_3$ is also turned on and $C_2$ is discharged in three

steps. Energy flows back to the source from $C_2$. The durations of the pulses applied to $SW_b$ are determined in such manner that the voltage of $C_2$ is decreased to $2Vs/3$, $Vs/3$, and 0 at $t_6$, $t_7$ and $t_8$, respectively. $C_1$ is not discharged toward input because $SW_1$ is off.

***Mode 4***

$SW_{C1}$ is turned off in mode 4. $C_1$ is discharged in the same manner as $C_2$ in mode 3. Meanwhile, $SW_{O4}$ is turned off and $SW_{O2}$ is turned on at $t_{11}$. The output section of the inverter becomes freewheeling state and reactive loading current is reset.

***Mode 5 to Mode 8***

$SW_{O1}$ is turned off and $SW_{O3}$ is turned on at the beginning of mode 5. The topologies of mode 5 to mode 8 are similar to that of mode 1 to mode 4 except that the polarity of the output voltage is reversed. Hence, the negative half-cycle is generated.

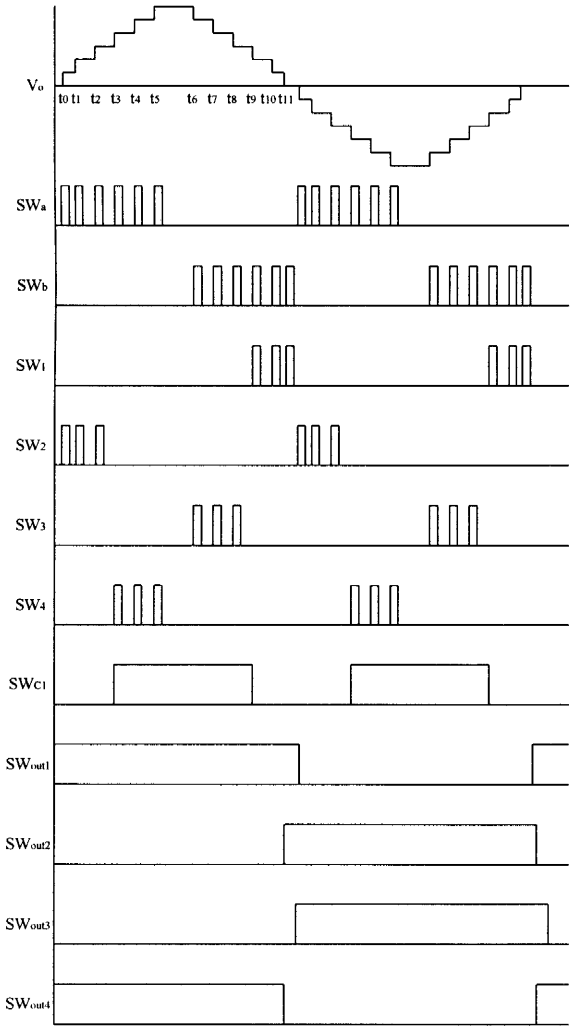
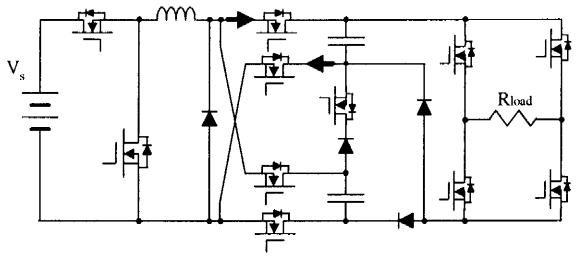
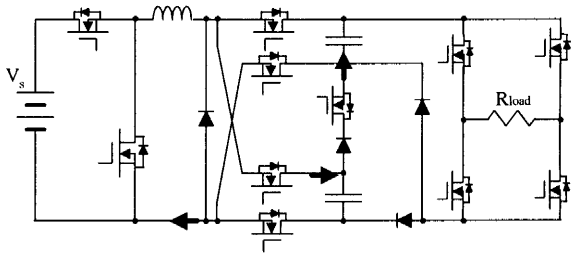


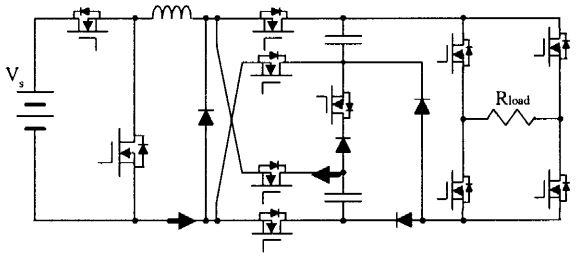

**Fig. 4** Timing diagram of output and switches



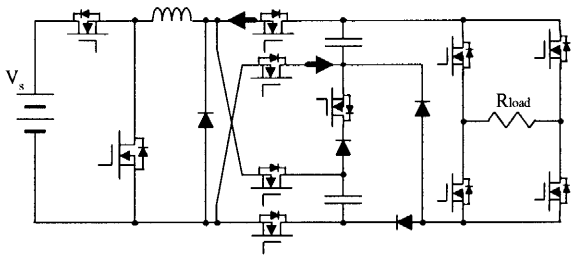

Mode 1




Mode 2




Mode 3




Mode 4

**Fig. 5** Switching topologies

## 4. DESIGN

The peak output voltage can be boosted up by increasing the number of capacitors, which is a function of the level of partial charging.

$$V_{O(peak)} = (kn - i)\frac{V_S}{k},\ i = 0,1,2,\ ...,\ kn \qquad (1)$$

$V_{O(peak)}$ and $V_S$ are the peak output voltage and input voltage, respectively. $n$ is the number of capacitors and $k$ is the level of partial discharging. $i$ is the level excluded from the switching sequence because it is necessary to fully charge all the capacitors.

If the inverter consists of two capacitors and each capacitor is charged to three different voltage levels, the

peak output voltage is a double of the input. However, the output voltage can be reduced by removing some of the gate pulses. For example, if the pulses at $t_5$ and $t_6$ are omitted, one voltage level can be reduced and the value of $i$ becomes 1. As a result, the peak output voltage is $5Vs/3$. Thus, the output voltage is adjustable by simply change the number of capacitors and level of partial charging.

The time intervals from $t_0$ to $t_{11}$ are not the same. The $j^{th}$ pulses starts at $t_j$ and the capacitor voltage will be $V_{c(j)}$. Since the capacitor voltage is equal to the sinusoidal output voltage, we have

$$Vc(j) = 2V_S \sin \omega t\,,\ j = 0,\ 1,\ 2,\ldots,\ 2nk\text{-}1 \qquad (2)$$

Since $Vc(j) = (j+1)\dfrac{V_S}{k}$ , it yields

$$t_j = \frac{1}{\omega}\sin^{-1}\left(\frac{j+1}{2k}\right) \qquad (3)$$

A series of pulses are applied to charge the capacitor from $t_0$ to $t_5$. When the inductance and equivalent series resistance are $L$ and $R_L$, respectively, and the capacitance is C with initial charge $V_{C(n-1)}$, the capacitor voltage can be expressed by

$$Vc(j+1) = \left[V_S - V_{C(j)}\right]\cdot\left(\frac{1}{4L-CR_L^2}\right)(4L-CR_L^2$$

$$+(CR_L^2-4L)\cos At\cdot e^{Bt} + \sqrt{C}R_L(4L-CR_L^2)\sin At\cdot e^{Bt}) \quad (4)$$

where

$$A = \frac{1}{2}\sqrt{\frac{4L-CR}{CL^2}}$$

$$B = \frac{R_L}{2L}$$

Substituting $V_C = V_S/3,\ 2V_S/3$, Vs into (4), we can determine the durations of the pulses.

Similarly, we can determine the pulse widths for discharging the capacitor from $t_6$ to $t_{11}$ by putting Vs=0 into (4).

## 5. RESULTS

The proposed PCSC inverter powered with 12V battery is developed. It consists of only two capacitors. The capacitance and inductance are 50μF and 100μH, respectively. There are three levels of partial charge, and the inverter is configured to generate 50Hz voltage. The circuit is simulated by using PSPICE and the results are shown in Figure 6. The output ac waveform closely follows a sinusoidal waveform.

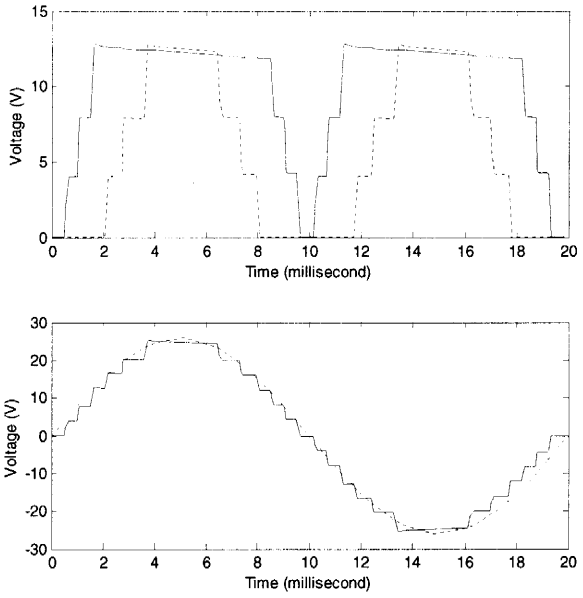



**Fig. 6** Simulation waveforms (upper trace: Capacitor voltage waveforms of $C_1$ (solid) and $C_2$ (dotted); lower trace: Output voltage waveform)

Experimental results of the capacitor voltages and output are shown in Figure 7 and Figure 8, respectively. The actual battery voltage is around 13.6V. Since the tolerances of the electrolytic capacitors are around 10%, the capacitor voltages deviate slightly from that of the simulation. On the other hand, the capacitors cannot be discharged completely to zero because the voltages drop across diodes and switches (MOSFET). However, the voltage is low and has little influence on the output. Both the simulation and experimental results verify the proposed inverter.

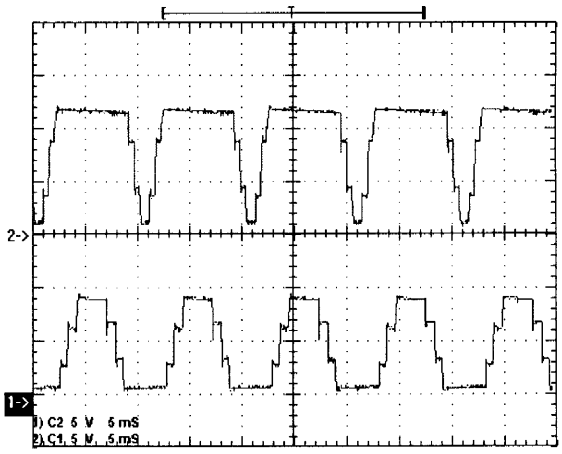


**Fig. 7** Experimental waveforms (upper trace: Voltage waveform of $C_1$; lower trace: Voltage waveform of $C_2$)

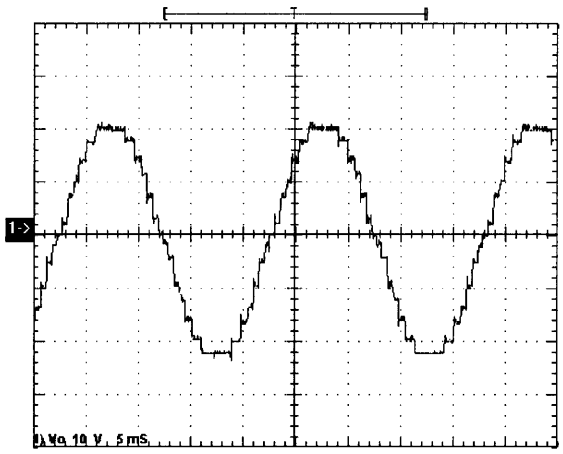


**Fig. 8** Experimental waveform of ac output voltage

## 7. CONCLUSION

A new SC inverter circuit based on partial charging has been developed. Without any transformer, the input voltage can be stepped up by the cascade of capacitors to generate an ac output with higher voltage. Low distortion output can be obtained with limited number of capacitors and switches. Moreover, the peak output voltage is adjustable by changing the levels of partial charging. Fewer capacitors imply lower production cost while more levels of partial charging reduce the output distortion without changing the stepping-up ratio. This inverter is very suitable for electric vehicles because it can generate a high ac voltage with the use of low voltage battery.

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