New Measuring Method for Battery Module's Voltage in Series Connected Battery Pack

Minxin Zheng [1], Bojin Qi [2], and Hongjie Wu [3]

[1] *Department of Mechanical Engineering and Automatic, Beijing University of Aeronautics and Astronautics, zhminxin@buaa.edu.cn*
[2] *Department of Mechanical Engineering and Automatic, Beijing University of Aeronautics and Astronautics, qbj@buaa.edu.cn*
[3] *Department of Mechanical Engineering and Automatic, Beijing University of Aeronautics and Astronautics, wuhj@buaa.edu.cn*

Abstract

The voltage of every battery module in series connected battery pack is important for diagnosing the battery pack, estimating the state of charge (SOC) of the pack and equalizing the pack in the battery management system (BMS). This paper introduces a method based CPLD for measuring the voltage of the battery module in series connected battery pack. The design and realization is also presented in detail. This method is already used successfully in BMS for EV and HEV.

Keywords

battery management system, battery module, measurement of voltage, CPLD

1. INTRODUCTION

The battery pack for EV and HEV is usually made up with as many as tens or hundreds of battery modules (cells) which are series connected. The battery modules may appear different status from each other because of the characteristics of itself or other reasons, so it is not proper to present the exact characteristics of the whole battery pack only by the total voltage of the whole battery pack. It is necessary that the battery management system (BMS) should get the information of every module for diagnosing the battery pack, determining the state of charge (SOC) of the battery pack and give advice for equalizing the battery pack by which the BMS let the battery pack work safely and maintain the battery pack's life.

2. HARDWARE DESIGH

It is difficult to adopt a normal method to sample every battery module at the same time because the battery modules are series connected and not the same "ground" during sampling [Jiang et al, 2000]. A new method of patrol sampling based on CPLD technique is presented in this paper. Only one battery module is connected to the sampling circuit at the same time through relays' array which is controlled by CPLD in this method. The relay used in this method is made up of photoMOS rated voltage is up to 400V.

The idea of this method is shown in Figure 1. It is obvious that the more battery modules the battery pack consists, the more I/O ports which control the relays are needed, but ordinary microprocessor (for example, 8x51) can not provide so many I/O ports. It is also noticeable

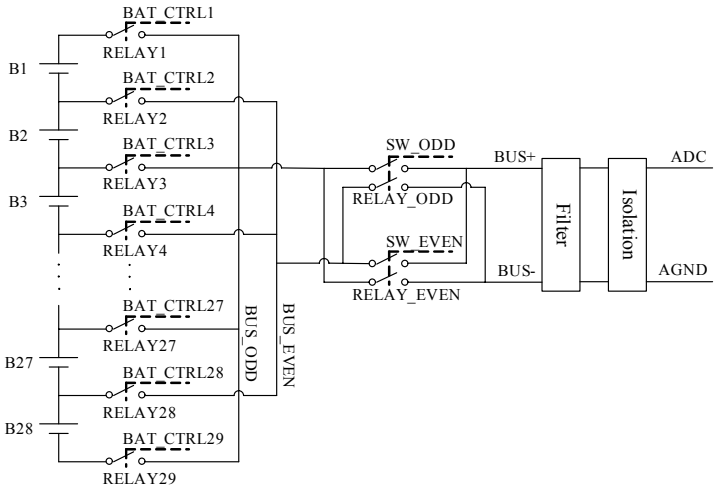

Fig. 1 Idea of patrol sampling

that the lose control of logic and schedule which control the relays is absolutely forbidden in this method otherwise the battery modules can be shorted through the sampling circuit. On account of all the above case, a reliable complex programmable logic device (CPLD) is used to control the relays in this method. Thus it is realizable that 2^n battery modules can be sampled only through n I/O ports of microprocessor via CPLD.

The CPLD this method adopts is MAX7128 [Altera, 1999] which is made by Altera Corporation and has 128 macros, 2500 logic gates, and 64 programmable I/O ports in itself. 52 battery modules can be sampled with this method via MAX7128. A sampling circuit system which can sample 28 battery modules is shown in Figure 2.

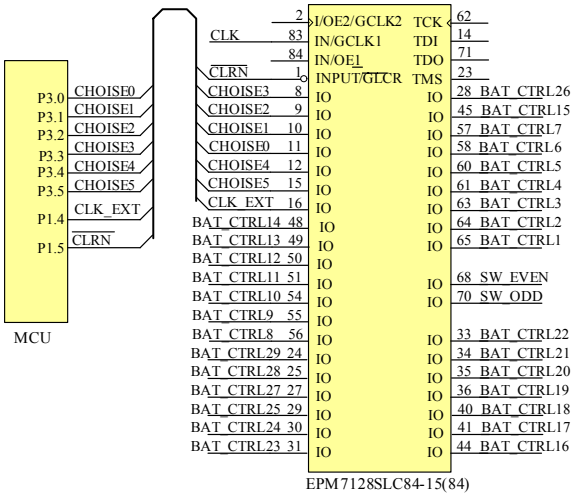

Fig. 2 Sampling circuit system with CPLD

The microprocessor gives the sequence number named CHOISE[5..0] through its 6 I/O ports named P3.5-P3.0, controlling signal named CLK_EXT through its I/O port named P1.4, enable signal named $\overline{\text{CLRN}}$ through its I/O port named P1.5. BAT_CTRL[29..1] signals which control the relays' array interpreted by CPLD. CLK signal which is a clock signal and generated by an oscillion is used to synchronize the output signal of CPLD.

3. SOFTWRE DESIGH

3.1 Design of CPLD

The software of the CPLD is designed by the Ahdl language based on the software named Max+plus II which is provided by Altera Corporation. When the microprocessor gives the sequence number CHOISE[5..0]=n and the enable signal CLK_EXT equals 1 (high level), the CPLD should interpret the output signals as follows: BAT_CTRL_n=1 and BAT_CTRL_{n+1}=1, SW_ODD1=1 if n is an odd or SW_EVEN1=1 if n is an even. Thus the corresponding relays are close and the nth battery module is connected to the sampling circuit. Then the voltage of this battery module is connected to the AD conversion unit after a lowpass filter and an isolation circuit. Considering the reliability of the system, D-trigger is adopted. The logic described in the Ahdl language is shown as following:

```
SUBDESIGN bat_ctrl_decoder
    (
    clk                 :INPUT;
    clk_ext             :INPUT;
    /clrn               :INPUT;
    choise[5..0]        :INPUT;
    bat_ctrl[29..1]     :OUTPUT;
    sw_odd              :OUTPUT;
    sw_even             :OUTPUT;
    )
    VARIABLE
    bat_ctrl_pre[29..1] :DFFE;
    sw_odd1_pre         :DFFE;
    sw_even1_pre        :DFFE;
    BEGIN
    sw_odd1_pre     = d[0];
    sw_even1_pre    = !d[0];
    TABLE
    choise[5..0]  =>    bat_ctrl_pre[29..1];
    1             =>    H"3";
    2             =>    H"6";
    3             =>    H"C";
    4             =>    H"18";
    •       =>  •
    •       =>  •
    •       =>  •
    27      =>  H"C000000";
    28      =>  H"18000000";
    END TABLE;
    bat_ctrl[]   = bat_ctrl_pre[].q;
    sw_odd1      = sw_odd1_pre.q;
    sw_even1     = sw_even1_pre.q;
    END;
```

A simulation is taken to this system with the Max+plusII and the result is shown in Figure 3. It can be seen that the output signal BAT_CTRL_5, BAT_CTRL_6 and EW_ODD1 are high level when input signal CHOISE[5..0] equals 5. Thus the fifth battery module is connected to the AD converting unit of microprocessor after the filter and the isolation circuit.

3.2 Design for reliability

The BMS may not work reliable when there exists strong electromagnetic disturbance during the EV or HEV is running. Some measure must be taken to resist these disturbances [Ma et al, 2004]. A π type of lowpass filter

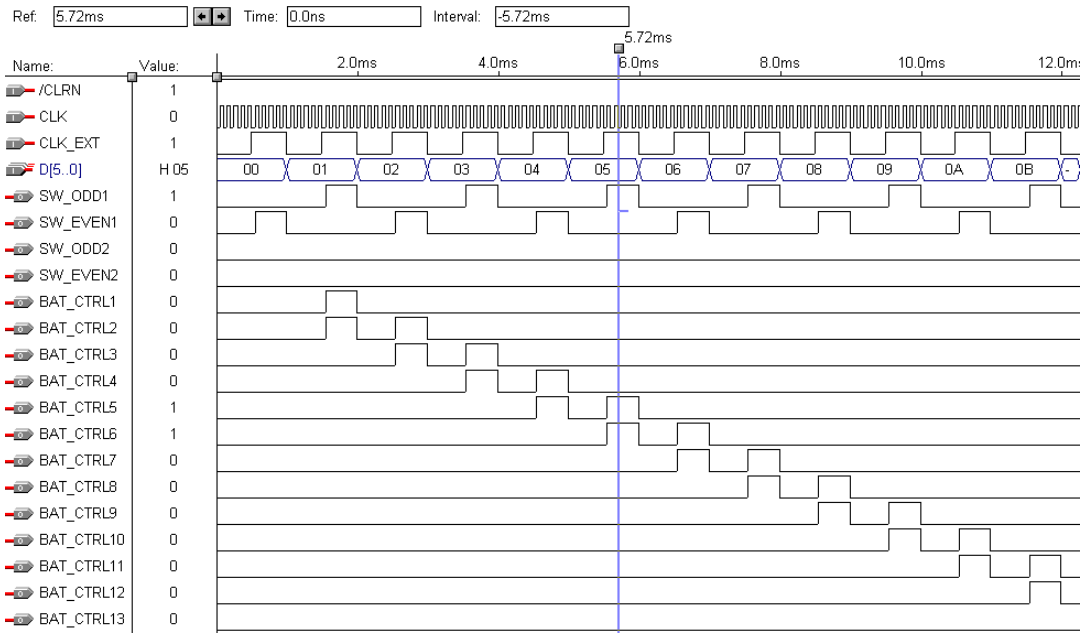

Fig. 3 Simulation of the design

and an isolation circuit used in the hardware design. An digital lowpass filter is also used as following:

$$y(n) = ay(n-1) + (1-a)s(n) \qquad (1)$$

Here $y(n-1)$ is the result of last time, $s(n)$ is the sampling value of this time, and a is the coefficient for filter. a is usually far less than 1. The less a is, the better the filter works but the more slowly the BMS responds. The BMS can work more reliable by these means. A photo from the oscillograph is shown in Figure 4 when the BMS is running.

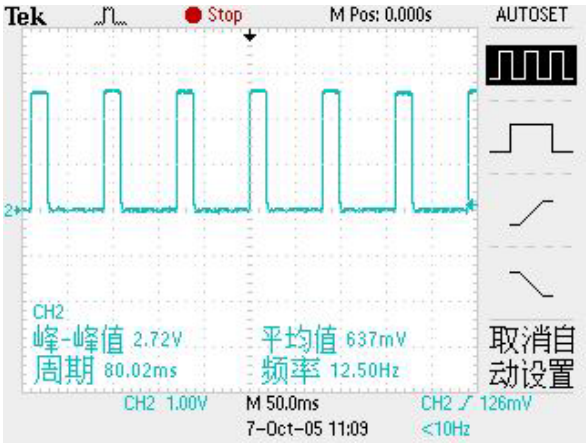

Fig. 4 Photo from the oscillograph

4. CONCLUSION

By the means of the patrol sampling based on the CPLD, the BMS can sample more battery modules with less I/O ports and run more reliably. This method has already used in our BMS for the EVs and HEVs.

References

Altera, Max 7000 Programmable Logic Device Family, www.altera.com, 1999.

Jiang, J., The Develop of Watching System by compter for EV, *Journal of Beijing University of Traffic*, Vol. 24, No. 3, 103-106, 2000.

Ma, J., The Battery Management System for EV Based on CAN, *Journal of Mechanical and Electronic Integrated*, No. 5, 62-65, 2004.

(Received April 11, 2007; accepted June 16, 2007)